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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,156	02/13/2004	Shuji Mayama	118678	4035

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OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
KITOV, ZEEV	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,156	MAYAMA ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1 - 12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 - 12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 July 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on December 17, 2004. Claims 1, 4, 7, 8, 9 and 11 are amended. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Izawa et al. (US 6,005,761). Regarding Claims 1 and 4, Izawa et al. disclose an FET as an N-channel MOS transistor (element 18 in Fig. 2) provided upstream of the load with respect to a flow of power current, the FET controlling an activation state of the load, the protection circuit including: a first connection changer (element 20 in Fig. 2) interposed on a connection line between a gate of the FET and a gate drive voltage supply source (elements 15 and 16 in Fig. 2), the first connection changer changing a connection state between a first connection state in which the gate is connected to the gate drive voltage supply and a second connection state in which the gate is connected to a ground (col. 14, line 65 24 – col. 15, line13); the first connection line connects a gate of the FET and a gate drive voltage supply source.

Regarding Claim 4, Izawa et al. disclose the first connection line as connecting a gate of the FET (element 18 in Fig. 2) and a gate drive voltage supply source (elements 15 and 16 in Fig. 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nasila (US 5,886,563) in view of Izawa et al. (US 6,005,761). Regarding Claims 1 and 4, Nasila discloses following elements: a circuit arrangement having an inductive load (col. 3, lines 15 – 20) and an FET as an N-channel MOS transistor (element Q1 in Fig. 3) provided upstream of the load with respect to a flow of power current, the FET controlling an activation state of the load, the protection circuit including: a first connection changer (element Q2 in Fig. 3) interposed on a connection line (elements R5 and CR3 in Fig. 3) between a gate of the FET and a gate drive voltage supply source (Vgg in Fig. 3), the first connection changer changing a connection state between a first connection state in which the gate is connected to the gate drive voltage supply and a second connection state in which the gate is connected to a ground (col. 5, lines 24 – 32); the first connection line connects a gate of the FET and a gate drive voltage supply source. However, Nasila circuit includes a zener diode (element CR2 in

Fig. 2). Izawa et al. disclose similar circuit (see rejection of Claim 1 under USC 102(b) above). The Izawa et al. circuit does not include the zener diode. A reason for that is that the zener diode in Nasila circuit is necessary only because it is half-bridge driver having two driving transistors. The zener diode helps to coordinate appropriate states of two transistors in the switching (col. 2, lines 9 – 16). Both references have the same problem solving area, namely providing power MOS load drivers. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Nasila solution by removing the second (bottom) transistor together with the zener diode from the circuit, since as well known in the art, the half-bridge drivers are used only for bipolar driving of the load, and if bipolar driving is not required, as Izawa et al. demonstrated, only one transistor and no zener diode is necessary. The Izawa circuit has definite advantage in cost of the parts.

Regarding Claim 2, Nasila discloses a first resistor (element R2 in Fig. 8) interposed between the gate and the source of the FET; and a second resistor interposed between the gate and the first connection changer (element R1 in Fig. 8).

Regarding Claim 9, it discloses the IGBT (element Q1 in Fig. 6).

Regarding Claim 11, it discloses the connection line (elements CR3 and R1 in Fig. 6) connecting a gate of the IGBT and a gate drive voltage supply source (Vgg in Fig. 6).

Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nasila in view of Izawa et al. As was stated above, Nasila and Izawa et al. disclose

all the elements of Claim 9. Regarding Claim 10, Nasila discloses a first resistor (element R2 in Fig. 8) interposed between the gate and the source of the FET and second resistor interposed between the connection changer (element Q2 in Fig.8) and the ground. It further discloses the IGBT (element Q1 in Fig. 6). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Nasila solution of Fig. 8 by replacing the FET by the IGBT, according to Fig. 6, because as Nasila states (col. 7, lines 25 – 27), the IGBT are popular in high voltage/current applications because of their low conduction losses.

Regarding Claim 12, Nasila discloses a first resistor (element R2 in Fig. 8) interposed between the gate and a source of the FET and a second resistor (element R1 in Fig. 8) interposed on a route from the gate of the FET to the ground through the connection line (element CR2 in Fig. 8) and the connection changer (element Q2 in Fig. 8). As to replacement of the FET by the IGBT, this issue was addressed above (see rejection of Claim 10).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nasila in view of Izawa et al. and Palara et al. (US 5,828,244). As was stated above, Nasila and Izawa et al. disclose all the elements of Claims 1 and 2. However, regarding Claim 3, they do not disclose a second connection changer interposed on a connection line between the gate and the source of the FET. Palara et al. disclose the second connection changer (element TR1 in Fig. 4) interposed on a connection line between the gate and the source of the FET (element M2 in Fig. 4). The connection changer

connects and disconnects the connection line between the gate and the source of the FET. It further discloses the first resistor (element R5 in Fig. 4) interposed on the connection line. Both references have the same problem solving area, namely providing a circuit for driving the MOS transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Nasila solution by adding the connection changer positioned on the connection line between the gate and the source of the FET, because as Palara et al. state (col. 5, line 65 – col. 6, line 5), to efficiently turn transistor off, a conduction path different from the one used for turning transistor on is to be used.

Claims 5, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nasila in view of Izawa et al. and Kitagawa et al. (US 6,392,463). As was stated above, Nasila and Izawa et al. disclose all the elements of Claim 4. Regarding Claim 5, Nasila further discloses a second resistor (elements R1, R2 in Fig. 3) interposed between the gate and the first connection changer. However, it does not disclose a first resistor interposed between the gate and a source of the FET. Kitagawa et al. disclose the first resistor (element R0 in Fig. 1) interposed between the gate and a source of the FET. Both references have the same problem solving area, namely providing a driving circuit for inductive loads. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Nasila solution by adding the resistor interposed between the gate and the source of the FET, because as Kitagawa et al. state (col. 1, lines 26 – 30), the resistor is necessary for reducing the

impedance between the gate and the source to stabilize the turning-on and turning-off operations of the MOS transistor. Additionally, the resistor would reduce the value of the voltage transient, which appears between the gate and the source due to inductive character of the load.

Regarding Claims 7 and 8, Nasila discloses the connection changer (element Q2 in Fig. 8) interposed between a portion on a connection line between a gate and a source of the FET (elements R1, and R2 in Fig. 8), and a ground (terminal Vss in Fig. 8), the connection changer connecting and disconnecting between the portion and the ground. It further discloses a first resistor (element R1 in Fig. 8) interposed on a route from the gate of the FET to the source thereof through the connection line. However, it does not disclose a p-channel MOS transistor. Kitagawa et al. disclose the p-channel MOS transistor (element Tr20 in Fig. 10) driving the inductive load (element 4 in Fig. 10). Both references have the same problem solving area, namely providing driving circuits for the inductive load. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Nasila solution by changing the n-channel MOS transistor for p-channel MOS transistor according to Kitagawa et al., because it is well known in the art, that the n-channel and p-channel MOS transistors are pretty close equivalents and mutually interchangeable, so selection of particular type of transistor is a matter of designer convenience.

As to a second resistor interposed between the gate and the drain of the FET, Kitagawa et al. disclose the first resistor (element R0 in Fig. 1) interposed between the gate and a source of the FET. Since in the circuit with the p-channel FET the transistor,

the terminal closest to the inductive load is the drain. By analogy, the drain – gate interface is to be treated the same way and protected the same way as the gate - source interface in the circuit with the n-channel FET, i.e. the resistor is to be placed between the gate and the drain. It is based on well known in the art fact, that the FET is symmetrically conducting element, therefore the drain and the source are to be treated similar way. Both references have the same problem solving area, namely providing the inductive load drivers. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Nasila solution by adding the resistor between the gate and the drain of the FET, because as Kitagawa et al. state because as Kitagawa et al. state (col. 1, lines 26 – 30), the resistor is necessary for reducing the impedance between the gate and the source (the gate and the drain) to stabilize the turning-on and turning-off operations of the MOS transistor. Additionally, the resistor would reduce the value of the voltage transient, which appears between the gate and the drain due to inductive character of the load.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nasila in view of Izawa et al., Kitagawa et al. and Palara et al. (US 5,828,244). As was stated above, Nasila, Izawa et al. and Kitagawa et al. disclose all the elements of Claims 4 and 5. However, regarding Claim 6, they do not disclose a second connection changer interposed on a connection line between the gate and the source of the FET. Palara et al. disclose the second connection changer (element TR1 in Fig. 4) interposed on a connection line between the gate and the source of the FET (element M2 in Fig. 4). The

connection changer connects and disconnects the connection line between the gate and the source of the FET. It further discloses the first resistor (element R5 in Fig. 4) interposed on the connection line. Both references have the same problem solving area, namely providing a circuit for driving the MOS transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Nasila solution by adding the connection changer positioned on the connection line between the gate and the source of the FET, because as Palara et al. state (col. 5, line 65 – col. 6, line 5), to efficiently turn transistor off, a conduction path different from the one used for turning transistor on is to be used.

Response to Arguments

Applicant's Arguments have been given careful consideration but they are moot in view of the new ground of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
03/04/2005

BRIAN S[illegible]
SUPERVISORY PA[illegible]
TECHNOLOGY C[illegible]